REMARKS:

In the outstanding final Office Action, claims 1-3 and 5-12 were rejected. Claims 1, 5, 8, 11 and 12 have been amended for clarification, and claims 3, 4, 7 and 10 have been cancelled without prejudice. Thus, claims 1, 2, 5, 6, 8, 9, 11 and 12 are pending and under consideration. No new matter has been added. The rejections are traversed below.

REJECTION UNDER 35 U.S.C. §102 (b):

At item 3 of the outstanding final Office Action, claims 1, 2, 5-6, 8-9 and 11-12 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,889,983 ('983).

'983 discusses a read-modify-write operation using a compare-and-exchange instruction implemented in an instruction set architecture of a computer system for acquiring access to a shared space within a memory.

The present invention discloses a method and circuit for controlling a semaphore and a processor using the same where a bus-arbitration control circuit is used to selectively assert a bus-arbitration acknowledge signal in response to a bus-arbitration request signal to prevent system inconsistency caused by memory access by other processors.

The Examiner compares the '983 compare-and-exchange operation that uses instruction sets to indicate an availability of a shared space within a memory with the present invention. In '983, a lock (or lock variable) is provided to a particular location in the memory, and a processor accesses the lock and tests a state (value) of the data stored therein to allow access to the shared space (see, column 4, lines 33-47 of '983). The memory address of where the lock value is located is loaded from the memory to a destination location, and a compare instruction is used to test the value of the lock (see, column 5, lines 35-37 of '983). If the comparison results in a true condition, the lock is in an unlocked state and vice versa if the comparison results in a false condition (see, column 5, lines 57-63 of '983). This means that the '983 operation is limited to comparing a lock value and a reference value to determine a state value of the lock.

As recited in each of the independent claims 1, 5, 8, 11 and 12 of the present invention, "a bus-arbitration control circuit which receives a signal indicative of a bus-arbitration request, the control signal, and a chip enable signal output from the processor" is provided to enable selective right of use where "... other resources are prohibited from accessing the semaphore address when the control signal is asserted, and a right to use a bus given to the processor is

not relinquished in response to the bus-arbitration request supplied from an external source during an asserted state of the control signal". Further, the bus-arbitration control circuit "asserts the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal when the chip enable signal is in a negated state and the control signal is in the negated state" and operates "not to assert a bus-arbitration-acknowledge signal in response to the bus-arbitration request signal regardless of a state of the chip enable signal when the control signal is in the asserted state... and when the chip enable signal is in an asserted state and the control signal is in a negated state". This allows the bus-arbitration control circuit to selectively assert a bus-arbitration-acknowledge signal in response to bus-arbitration requests.

It is submitted that each of the independent claims are patentable over '983.

For at least the above-mentioned reasons, claims depending from independent claims 1, 5, 8, 11 and 12 are patentably distinguishable over '983. The dependent claims are also independently patentable. For example, as recited in claims 2, 6 and 9, the present invention includes, "a comparator which makes a comparison of an address output from the processor with the semaphore address stored in said register, and asserts a match signal when the comparison indicates a match" where asserted and negates states are set in response to an assertion of a match control signal. The '983 method does not teach or suggest comparing the address output from the processor with the semaphore address stored in said register and setting the control signal to asserted/negated states based on which a bus-arbitration control circuit operates to assert and/or not to assert a bus-arbitration acknowledge signal.

Therefore, withdrawal of the rejection is respectfully requested.

CONCLUSION:

In accordance with the foregoing, claims 1, 5, 8, 11 and 12 have been amended, and claims 3, 4, 7 and 10 have been cancelled without prejudice. Thus, claims 1, 2, 5, 6, 8, 9, 11 and 12 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

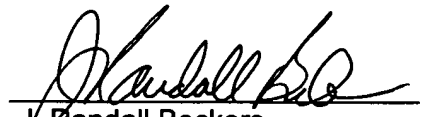
Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 8/30/04

By: 

J. Randall Beckers
Registration No. 30,358

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 454-1589
Facsimile: (202) 434-1501